July 2008

# FDW254PZ

## P-Channel 1.8V Specified PowerTrench® MOSFET

### General Description

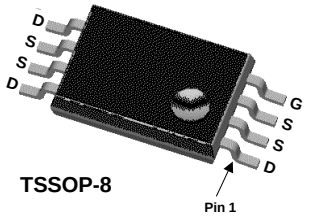
This P-Channel 1.8V specified MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications with a wide range of gate drive voltage (1.8V – 8V).

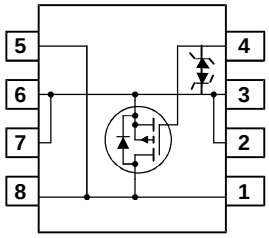
### Applications

- Load switch
- Motor drive
- DC/DC conversion
- Power management

### Features

- –9.2 A, –20 V. $R_{DS(ON)}$ = 12 mΩ @ $V_{GS}$ = –4.5 V
  $R_{DS(ON)}$ = 15 mΩ @ $V_{GS}$ = –2.5 V
  $R_{DS(ON)}$ = 21.5 mΩ @ $V_{GS}$ = –1.8 V
- Rds ratings for use with 1.8 V logic
- ESD protection diode
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$
- Low profile TSSOP-8 package




## Absolute Maximum Ratings

$T_A$=25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | –20 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±8 | V |
| $I_D$ | Drain Current – Continuous | (Note 1) | –9.2 | A |
| | – Pulsed | | –50 | |
| $P_D$ | Power Dissipation | (Note 1a) | 1.4 | W |
| | | (Note 1b) | 1 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +150 | °C |

## Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 96 | °C/W |
| | | (Note 1b) | 208 | |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| 254PZ | FDW254PZ | 13'' | 12mm | 2500 units |

## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = –250 µA | –20 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = –250 µA, Referenced to 25°C | | –11 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = –16 V, $V_{GS}$ = 0 V | | | –1 | µA |
| $I_{GSS}$ | Gate–Body Leakage | $V_{GS}$ = ±8 V, $V_{DS}$ = 0 V | | | ±10 | µA |
| **On Characteristics** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = –250 µA | –0.4 | –0.6 | –1.5 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = –250 µA, Referenced to 25°C | | 2 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = –4.5 V, $I_D$ = –9.2 A<br>$V_{GS}$ = –2.5 V, $I_D$ = –7.9 A<br>$V_{GS}$ = –1.8 V, $I_D$ = –6.5 A<br>$V_{GS}$=–4.5 V, $I_D$ =–9.2 A, $T_J$=125°C | | 9<br>11<br>14<br>12 | 12<br>15<br>21.5<br>18 | mΩ |
| $I_{D(on)}$ | On–State Drain Current | $V_{GS}$ = –4.5 V, $V_{DS}$ = –5 V | –50 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = –5 V, $I_D$ = –9.2 A | | 54 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = –10 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 5880 | | pF |
| $C_{oss}$ | Output Capacitance | | | 990 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 560 | | pF |
| $R_G$ | Gate Resistance | $V_{GS}$ = 15 mV, f = 1.0 MHz | | 4.9 | | Ω |
| **Switching Characteristics** (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = –10 V, $I_D$ = –1 A, $V_{GS}$ = –4.5 V, $R_{GEN}$ = 6 Ω | | 15 | 27 | ns |
| $t_r$ | Turn–On Rise Time | | | 15 | 27 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 210 | 336 | ns |
| $t_f$ | Turn–Off Fall Time | | | 100 | 160 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = –10 V, $I_D$ = –9.2 A, $V_{GS}$ = –4.5 V | | 60 | 96 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | 7 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | 13 | | nC |
| **Drain–Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | | | –1.2 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = –1.2 A (Note 2) | | –0.5 | –1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = –9.2 A, $d_{iF}/d_t$ = 100 A/µs | | 35 | | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 21 | | nC |

**Notes:**

**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) $R_{\theta JA}$ is 96°C/W (steady state) when mounted on a 1 $inch^2$ copper pad on FR-4.

b) $R_{\theta JA}$ is 208°C/W (steady state) when mounted on a minimum copper pad on FR-4.

2. Pulse Test: Pulse Width < µs, Duty cycle < 2.0%.

## Typical Characteristics

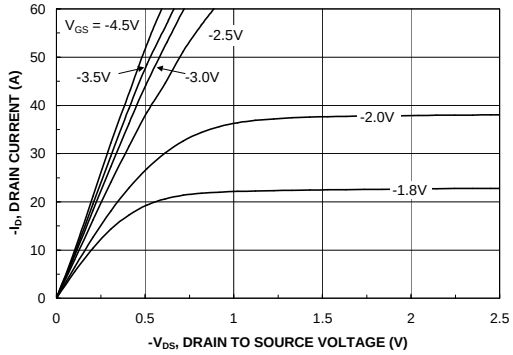



**Figure 1. On-Region Characteristics.**

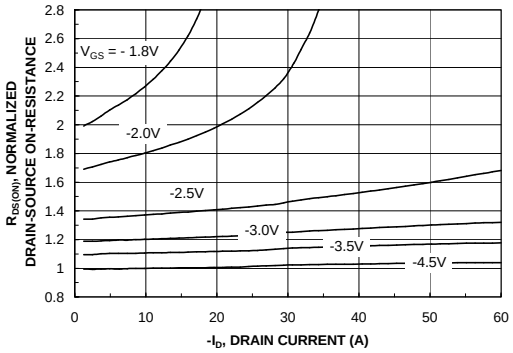



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

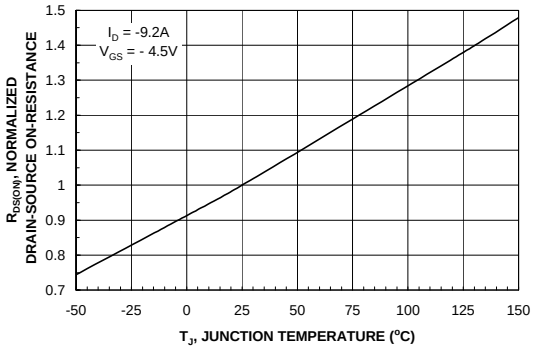



**Figure 3. On-Resistance Variation withTemperature.**

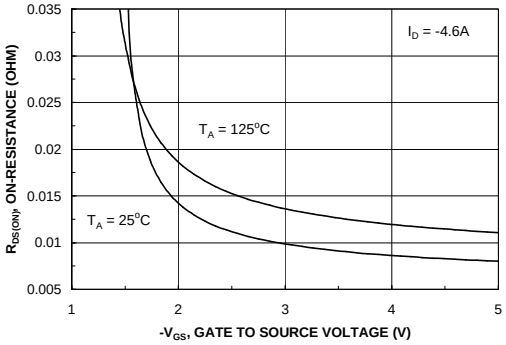



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

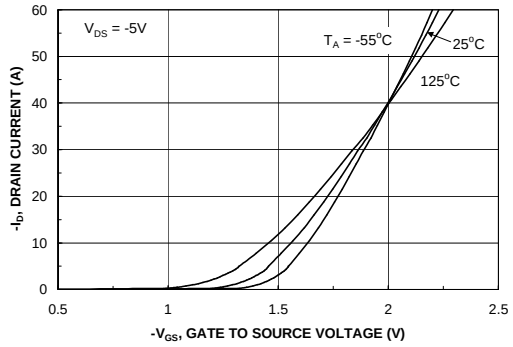



**Figure 5. Transfer Characteristics.**

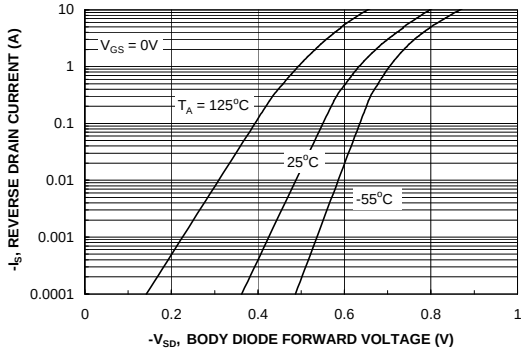



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics

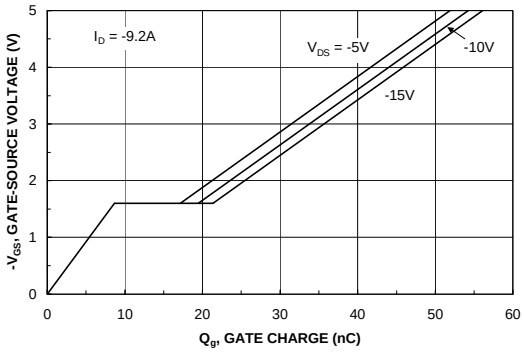



**Figure 7. Gate Charge Characteristics.**

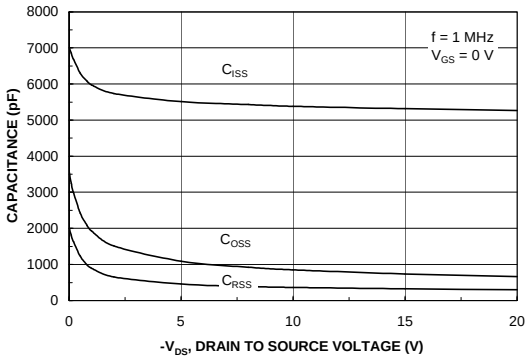



**Figure 8. Capacitance Characteristics.**

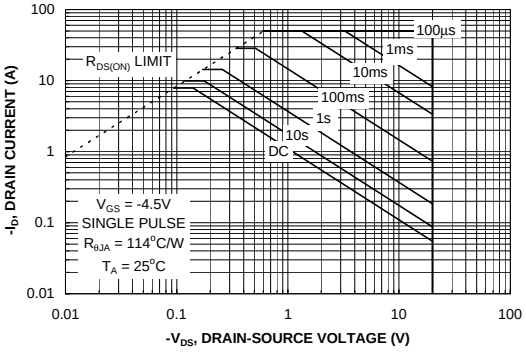



**Figure 9. Maximum Safe Operating Area.**

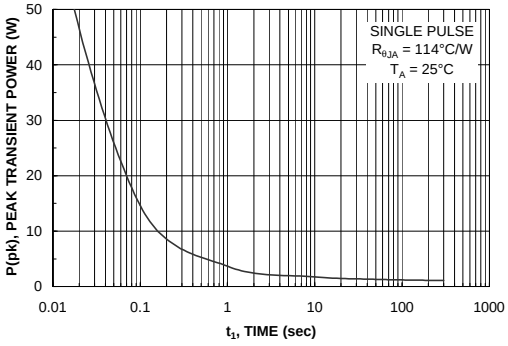



**Figure 10. Single Pulse Maximum Power Dissipation.**

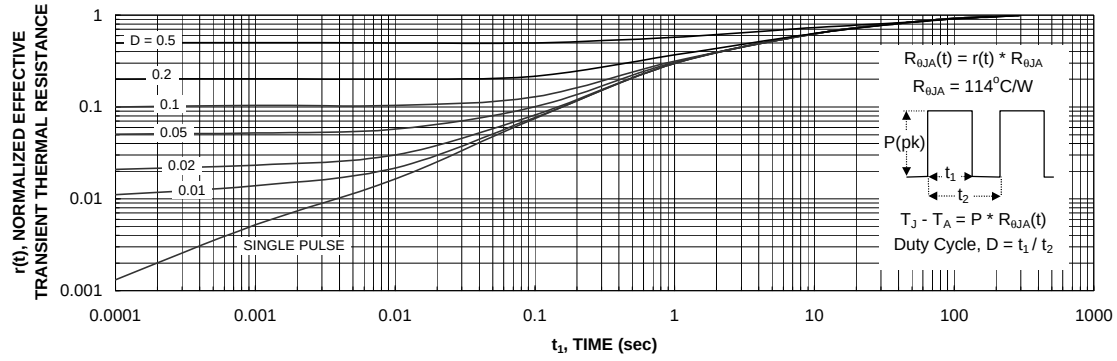



**Figure 11. Transient Thermal Response Curve.**

**Thermal characterization performed using the conditions described in Note 1b.**
**Transient thermal response will change depending on the circuit board design.**

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